Michael J. Wirthlin

Professor
Department of Electrical and Computer Engineering
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Education:

Ph.D. Brigham Young University, Provo, UT - Electrical and Computer Engineering
Dissertation: Improving Functional Density Through Run-Time Circuit Reconfiguration
August 1997

B.S. Brigham Young University, Provo, UT - Electrical and Computer Engineering
August 1992, Suma Cum Laude with University Honors
Honors Thesis: A Quantitative Study of RISC Pipelining Techniques Using Custom Software Simulation Tools

Areas of Specialization:

FPGA Reliability
Digital Circuit Design
FPGA Circuit Design
High-Level Synthesis
Single-Event Effects Testing
Computer System Reliability
Reconfigurable Computing Architectures
Application-Specific Computing Architectures
Reliable Computing
Fault-Tolerant Computing

Professional Experience:

Assistant, Associate, and Full Professor (1999 – present)
Dept. of Electrical and Computer Engineering, Brigham Young University, Provo, UT

Intellectual Property Legal Consultant (2004-2005, 2011-2013, 2015-2016)
Pia Anderson Dorius Reynard & Moss, Salt Lake City, UT
Maschoff Brennan, Salt Lake City, UT
Workman Nydegger, Salt Lake City, UT
Irell and Manella, LLP, Los Angeles, CA

- Review patents in computer architecture, hardware design, and software systems
- Testify in patent litigation and intellectual property disputes

Staff Engineer (1997-1998)
National Semiconductor, Architecture Laboratory, Santa Clara, CA

- Investigate and develop system design methodologies for single-chip systems
- Create system performance modeling for embedded system on chip architectures

Design Engineer (1992-1994)
National Technology Incorporated, Salt Lake City, UT

- FPGA design of digital sound products
- Configurable computing architecture development

Controls Engineer, Co-Op (1990-1991)
Saturn Corporation, Lost Foam and Vehicle Systems Operations, Spring Hill, TN

- PLC programmer for automobile manufacturing facility

Professional Activities

Senior Member of the IEEE, member of IEEE Computer Society
Member of the Association for Computing Machinery (ACM), Tau Beta Pi
Program Session Organizer, IEEE Nuclear and Space Radiation Effects Conference, 2017
Chair and organizer of the Soft-Errors and Programmable Logic (SEPL) Workshop, 2016
Publications Chair for the Military Aerospace Programmable Logic Devices (MAPLD) Workshop, 2014
Program Co-Chair for the International Conference on Reconfigurable Computing and FPGAs (ReConFig 2013-2014),
Technical Co-Chair for the Military Aerospace Programmable Logic Devices (MAPLD) Workshop, April 2013
General Chair for the International IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM 2011)
Technical Program Co-Chair for the International IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM 2010)
Technical program committee and publicity chair for International Conference on Field Programmable Logic and Applications (FPL 2008-2009)
Reviewer for *IEEE Transactions on VLSI Systems*, *Kluwer Journal of VLSI Signal Processing*, *IEEE Computer Magazine*, ACM Design Automation Conference, IEEE Symposium on Field-Programmable Custom Computing Machines, IEEE Transactions on Computers, and the International Symposium on Signal Processing and its Applications (ISSPA).
Review panelist for the National Science Foundation
Technical program committee for ACM/SIGDA International Symposium on Field-Programmable Gate Arrays, International conference on Engineering of Reconfigurable Systems and Algorithms, and International Conference on Military and Aerospace Programmable Logic Devices (MAPLD).
Special session organizer (Reconfigurable System on Chip Architectures), International conference on Engineering of Reconfigurable Systems and Algorithms (2004)
Member of ACM/SIGDA DAC PhD forum organizing committee (2002-2004)

Educational Responsibilities

Department ABET and Assessment Coordinator (2013 – present)
Department graduate coordinator (2006 – 2010)
University Sailing Club Advisor (2004 – 2009)

Awards:

Ira Fulton College of Engineering and Technology Excellence in Research Award, 2017
Ira Fulton College of Engineering and Technology Excellence in Citizenship Award, 2010
Outstanding Faculty Award, Dept. of Electrical and Computer Engineering, 2007
Faculty advisor to 3rd place at IEEE Computer Society International Design Competition, 2001

Courses Taught:

ECEN 220/224: Introductory Digital Design and State Machines
ECEN 320: Advanced Digital Design
ECEN 323: Computer Organization
ECEN 427: Embedded Systems

ECEN 490: Senior Project (Computer System Design Project, FPGA Software Radio Project)
ECEN 523: Computer System Reliability
ECEN 528: Advanced Computer Architecture
ECEN 625: Synthesis and Optimization of Digital Circuits
ECEN 523: Computer System Reliability

Courses Developed:

Computer Organization: Developed a new sequence of digital design laboratories leading students through the design of a simplified MIPs microprocessor.
Introduction to Digital Systems Laboratory: Developed a new sequence of twelve digital design laboratories based on the most recent design tools and digital logic systems.
Computer System Reliability: Developed a new three credit hour graduate course that includes reliability modeling concepts and fault tolerant computer system design techniques.
Advanced Digital Design Course: Developed a new five credit hour junior level digital design course to include relevant topics and more advanced material.
Advanced Digital Design Laboratory: Initiated the use of FPGAs in undergraduate teaching laboratories. Organized laboratory sequence for students to design and test a simple 16-bit processor.
Synthesis and Optimization of Digital Circuits: Introduced a new graduate course on digital circuit synthesis with an emphasis on scheduling and resource sharing.
Computer Systems Senior Project: Introduced a new senior project involving the specification, design, and testing of a complete computer system (hardware and software). Students taking this class participated in the IEEE Computer Society International Design Competition (CSIDC) and placed 3rd in the 2001 finals in Washington D.C.

Publications:

Journal Publications

1. Andrew Keller, Timothy Whiting, Kenneth Sawyer, and Michael Wirthlin, "Dynamic SEU Sensitivity of Designs on Two 28-nm SRAM-based FPGA Architectures", *IEEE Transactions on Nuclear Science*, vol. 65, no. 1, pp. 280-287, Jan. 2017.
2. M. Brusati, A. Camplani, M. Cannon, H. Chen, M. Citterio, M. Lazzaroni, H. Takai, M. Wirthlin, "Mitigated FPGA design of multi-gigabit transceivers for application in high radiation environments of High Energy Physics experiments," *Measurement,* vol. 108, pp. 171-192, October 2017.
3. Aaron Stoddard, Aaron Gruwell, and Michael Wirthlin, "A Hybrid Approach to FPGA Configuration Scrubbing in High-Radiation Environments", *IEEE Transactions on Nuclear Science*, vol. 64, no. 1, pp. 497-503, Jan. 2017.
4. Andrew Keller and Michael Wirthlin, "Benefits of Complementary SEU Mitigation for the LEON3 Soft Processor on SRAM-based FPGAs", *IEEE Transactions on Nuclear Science*, vol. 64, no. 1, pp. 519-528, Jan. 2017.
5. M. Citterio, A. Camplani, M. Cannon, H. Chen, K. Chen, B. Deng, C. Liu, C. Meroni, J. Kierstead, H. Takai, M. Wirthlin, and J. Ye, "Radiation testing campaign results for understanding the suitability of FPGAs in detector electronics," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment,* vol. 824, pp. 270-271, July 11, 2016. doi:10.1016/j.nima.2015.11.033
6. N.A. Dodds, M.J. Martinez, P.E. Dodd, M.R. Shaneyfelt, F.W. Sexton, J.D. Black, D.S. Lee, S.E. Swanson, B.L. Bhuva, K.M. Warren, R.A. Reed, J. Trippe, B.D. Sierawski, R.A. Weller, N. Mahatme, N.J., Gaspard, T. Assis, R. Austin, S.L. Weeden-Wright, L.W. Massengill, G. Swift, M. Wirthlin, M. Cannon, R. Liu, L. Chen, A.T. Kelly, P.W. Marshall, M. Trinczek, E.W. Blackmore, S.-J. Wen, R. Wong, B. Narasimham, J.A. Pellish, and H. Puchner "The Contribution of Low-Energy Protons to the Total On-Orbit SEU Rate," *IEEE Transactions on Nuclear Science* , vol. 62, no. 6, pp. 2440–2451, Dec. 2015. (**Best Paper Award**)

7. D.S. Lee, G.M. Swift, M.J. Wirthlin, and J. Draper, "Addressing Angular Single-Event Effects in the Estimation of On-Orbit Error Rates," *IEEE Transactions on Nuclear Science,* vol.62, no.6, pp. 2563-2569, Dec. 2015.
8. M. Cannon, M. Wirthlin, A. Camplani, M. Citterio, and C. Meroni, "Evaluating Xilinx 7 Series GTX Transceivers for Use in High Energy Physics Experiments Through Proton Irradiation," *IEEE Transactions on Nuclear Science*, vol. 62, no. 6, pp. 2695-2702, Dec. 2015.
9. H. Quinn, W.H. Robinson, P. Rech, M. Aguirre, A. Barnard, M. Desogus, L. Entrena, M. Garcia-Valderas, S.M. Guertin, D. Kaeli, F. Lima Kastensmidt, B.T. Kiddie, A. Sanchez-Clemente, M. Sonza Reorda, L. Sterpone, M. Wirthlin, "Using Benchmarks for Radiation Testing of Microprocessors and FPGAs," *IEEE Transactions on Nuclear Science,* vol.62, no.6, pp.2547-2554, Dec. 2015.
10. H. Quinn, and M. Wirthlin, "Validation Techniques for Fault Emulation of SRAM-based FPGAs," in *IEEE Transactions on Nuclear Science,* vol. 62, no. 4, pp.1487-1500, Aug. 2015.
11. M. Wirthlin, "High-Reliability FPGA-Based Systems: Space, High-Energy Physics, and Beyond," in *Proceedings of the IEEE*, vol.103, no.3, pp.379-389, March 2015.
12. Heather Quinn, Diane Roussel-Dupre, Mike Caffrey, Paul Graham, Michael Wirthlin, Keith Morgan, Anthony Salazar, Tony Nelson, Will Howes, Eric Johnson, Jon Johnson, Brian Pratt, Nathan Rollins, and Jim Krone, "The Cibola Flight Experiment," *ACM Trans. Reconfigurable Technol. Syst.* Volume 8, Issue 1, Article 3 (March 2015), 22 pages. 2015 (**Best article of 2015 award**).
13. M. Wirthlin, D. Lee, G. Swift, H. Quinn, "A Method and Case Study on Identifying Physically Adjacent Multiple-Cell Upsets Using 28-nm, Interleaved and SECDED-Protected Arrays," *IEEE Transactions on Nuclear Science*, vol. 61, no. 6, pp.3080-3087, Dec. 2014
14. Michael Wirthlin, Helio Takai, and Alex Harding, "Soft Error rate estimations of the Kintex-7 FPGA within the ATLAS Liquid Argon (LAr) Calorimeter"*, IOP Science Journal of Instrumentation*, Vol. 9, No. C01025, January 2014.
15. Quinn, H.; Graham, P.; Morgan, K.; Baker, Z.; Caffrey, M.; Smith, D.; Wirthlin, M.; Bell, R., "Flight Experience of the Xilinx Virtex-4, " Nuclear Science, IEEE Transactions on, vol. 60, no. 4, pp. 2682-2690, Aug. 2013.
16. Michael Wirthlin, "FPGAs operating in a radiation environment: lessons learned from FPGAs in space"*, IOP Science Journal of Instrumentation*, Vol. 8, No. C02020, February 2013.
17. Brian Pratt, Megan Fuller, Michael Rice, and Michael Wirthlin, "Reduced-Precision Redundancy for Reliable FPGA Communications Systems in High-Radiation Environments", *IEEE Transactions on Aerospace and Electronic Systems*, Vol. 49, No. 1, pp. 369—379, January 2013.
18. Brian Pratt, Megan Fuller, and Michael Wirthlin, "Reduced-Precision Redundancy on FPGAs", *International Journal of Reconfigurable Computing*, Vol. 2011, 12 pages, Oct. 2011.
19. Yubo Li, Brent Nelson, and Michael Wirthlin, "Synchronization Techniques for Crossing Multiple Clock Domains in FPGA-Based TMR Circuits", *IEEE Transactions on Nuclear Science*, Vol. 57, No. 6, pp. 3506 - 3514, December 2010.
20. A. Propst, K. Peters, M. A. Zikry, S. Schultz, W. Kunzler, Z. Zhu, M. Wirthlin, R. Selfridge, "Assessment of damage in composite laminates through dynamic, full-spectral interrogation of fiber Bragg grating sensors", *Smart Materials and Structures*, Vol 19, Structures and Materials, p. 1-11, January 2010.
21. Patrick Ostler, Michael P. Caffrey, Derrick Gibelyou, Paul S. Graham, Keith S. Morgan, Brian H. Pratt, Heather M. Quinn, and Michael J. Wirthlin, "SRAM FPGA Reliability Analysis for Harsh Radiation Environments", *IEEE Transactions on Nuclear Science (NSREC)*, Vol. 56, No. 6, pp. 3519-3526, December 2009.
22. Heather Quinn, Paul Graham, Michael Wirthlin, Brian Pratt, Keith Morgan, Michael Caffrey, and Jim Krone, "A Test Methodology for Determining Space-Readiness of Xilinx SRAM-based FPGA Devices and Designs", *IEEE Transactions on Instrumentation and Measurement*, Vol. 58, No. 10, pp. 3380-3395, October 2009.
23. S. Schultz, W. Kunzler, Z. Zhu, M. Wirthlin, R. Selfridge, A. Propst, M. Zikry and K. Peters, "Full-spectrum interrogation of fiber Bragg grating sensors for dynamic measurements in composite laminates," *Smart Materials and Structures*, vol. 18, p. 115015, Sept. 2009.
24. Brian Pratt, Michael Caffrey, James F. Carroll, Paul Graham, Keith Morgan, and Michael Wirthlin, "Fine-Grain SEU Mitigation for FPGAs Using Partial TMR", *IEEE Transactions on Nuclear Science*, Vol. 55, No. 4, pp. 2274-2280, August 2008.
25. M. Wirthlin, D. Poznanovic, P. Sundararajan, A. Coppola, D. Pellerin, W. Najjar, R. Bruce, M. Babst, O. Pritchard, P. Palazzari, G. Kuzmanov, "OpenFPGA CoreLib Core Library Interoperability Effort", *Journal of Parallel computing*, Vol. 34, No. 4-5, pp. 231-244. 2008.
26. Brent E. Nelson, Brad L. Hutchings, and Michael J. Wirthlin, "Design, Debug, Deploy: The Creation of Configurable Computing Applications", *Journal of Signal Processing Systems*, Vol. 53, No. 1-2, pp. 187-196. 2008.
27. Keith Morgan, Daniel McMurtrey, Brian Pratt, and Michael Wirthlin, "A Comparison of TMR With Alternative Fault-Tolerant Design Techniques for FPGAs", *IEEE Transactions on Nuclear Science*, Vol. 54, No. 6, Part 1, pp. 2065 - 2072, December 2007.

28. Welson Sun, Michael J. Wirthlin, and Stephen Neuendorffer, "FPGA Pipeline Synthesis Design Exploration Using Module Selection and Resource Sharing", *IEEE Transactions on Computer Aided Design*, Vol. 26, No. 2, pp. 254-265, February 2007.
29. Maya Gokhale, Paul Graham, Michael Wirthlin, D. Eric Johnson, and Nathaniel Rollins, "Dynamic Reconfiguration for Management of Radiation-Induced Faults in FPGAs", *International Journal of Embedded Systems*, Vol. 2, No. 1/2, pp. 28-38, 2006.
30. Keith Morgan, Michael Caffrey, Paul Graham, Eric Johnson, Brian Pratt, and Michael Wirthlin, "SEU-Induced Persistent Error Propagation in FPGAs", *IEEE Transactions on Nuclear Science*, Vol. 52, No. 6, Part 1, pp. 2438 - 2445, December 2005.
31. D. Eric Johnson, Michael Caffrey, Paul Graham, Nathan Rollins, and Michael Wirthlin, "Accelerator Validation of an FPGA SEU Simulator", *IEEE Transactions on Nuclear Science*, Vol. 50, No. 6, pp. 2147-2157, December 2003.
32. Paul Graham, Michael Caffrey, D. Eric Johnson, Nathan Rollins, and Michael Wirthlin, "SEU Mitigation for Half-Latches in Xilinx Virtex FPGAs", *IEEE Transactions on Nuclear Science*, Vol. 50, No. 6, pp. 2139-2146, December 2003.
33. Michael J. Wirthlin, "Constant Coefficient Multiplication Using Look-up Tables", *Journal of VLSI Signal Processing*, Vol. 36, pp. 7-15, 2004.
34. Edward A. Lee, Stephen Neuendorffer, and Michael J. Wirthlin, "Actor-Oriented Design of Embedded Hardware and Software Systems", Invited paper to the *Journal of Circuits, Systems, and Computer,* Vol. 12, No. 3, pp. 231-260, June 2003.
35. Michael J. Wirthlin and Brian McMurtrey, "Web-Based IP Evaluation and Distribution Using Applets", *IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems,* Vol. 22, No. 8, pp. 985-994, August 2003.
36. B. L. Hutchings, B. Nelson and M. J. Wirthlin, "Designing and Debugging Custom Computing Applications", *IEEE Design and Test of Computers*, Vol. 17, No. 1, pp. 20-28, January 2000.
37. M. J. Wirthlin and B.L. Hutchings, "Improving Functional Density Using Run-Time Circuit Reconfiguration", *IEEE Transactions on VLSI Systems*, vol. 6, no. 2, pp. 247-256, 1998.

Book Chapters

1. Alex Harding and Michael J. Wirthlin "Hybrid Configuration Scrubbing for Xilinx Series-7 FPGAs," Chapter 6 of FPGAs and Parallel Architectures for Aerospace Applications, pp. 61-74, Springer, 2016.
2. Nathan Harward, Michael Gardiner, Luke Hsiao, and Michael J. Wirthlin "A Fault Injection System for Measuring Soft Processor Design Sensitivity on Virtex-5 FPGAs," Chapter 7 of FPGAs and Parallel Architectures for Aerospace Applications, pp. 91-101, Springer, 2016.
3. Heather M. Quinn, Keith S. Morgan, Paul S. Graham, James B. Krone, Michael P. Caffrey, Kevin Lundgreen, Brian Pratt, David Lee, Gary M. Swift, Michael J. Wirthlin "Assuring Robust Triple-Modular Redundancy Protected Circuits in SRAM-Based FPGAs," Chapter 8 of Ionizing Radiation Effects in Electronics: From Memories to Imagers, CRC Press, pp. 195-228, 2015.
4. Keith S. Morgan, Los Alamos National Laboratory, James Carroll, Michael Caffrey, Derrick Gibelyou, Paul Graham, William Howes, Jonathan Johnson, Daniel McMurtrey, Patrick Ostler, Brian Pratt, Heather Quinn, Michael Wirthlin, "Fault Tolerance Techniques and Reliability Modeling for SRAM-based FPGAs", Chapter in Radiation Effects in Semiconductors: Devices, Circuits, and Systems, CRC Press, 2010.

Conference Publications, Full Paper Peer Review

1. B. Hutchings and M. Wirthlin, "Rapid implementation of a partially reconfigurable video system with PYNQ", *Proceedings of the 27th International Conference on Field Programmable Logic and Applications (FPL-2017)*, September 2017, pp. 1-8, DOI: 10.23919/FPL.2017.8056845
2. David S. Lee, Gary Swift, and Michael Wirthlin, "An Analysis of High-Current Events Observed on Xilinx 7-Series and UltraScale Field- Programmable Gate Arrays," *2016 IEEE Radiation Effects Data Workshop (REDW)*, pp.1-5, Dec. 2016.
3. Ammon Gruwell, Peter Zabriskie, and Michael Wirthlin, "High-Speed FPGA Reliability Testing Over JTAG", *IEEE AUTOTESTCON 2016*, September, 2016, pp. 1-8, DOI: 10.1109/AUTEST.2016.7589601

4. Aaron Stoddard and Michael Wirthlin, "High-speed PCAP configuration scrubbing on Zynq-7000 All Programmable SoCs", *Proceedings of the 26th International Conference on Field Programmable Logic and Applications (FPL-2016)*, September 29, 2016, pp. 1-8, DOI: 10.1109/FPL.2016.7577301
5. Luke Newmeyer, Michael J. Wirthlin, Doran Wilde, and Brent Nelson, "Efficient Processing of Phased Array Radar in Sense and Avoid Application Using Heterogeneous Computing", *Proceedings of the 26th International Conference on Field Programmable Logic and Applications (FPL-2016)*, September 29, 2016, pp. 1-8, DOI: 10.1109/FPL.2016.7577322
6. Ammon Gruwell, Peter Zabriskie, Michael J. Wirthlin, "High-speed programmable FPGA Configuration through JTAG", *Proceedings of the 26th International Conference on Field Programmable Logic and Applications (FPL-2016)*, September 29, 2016, pp. 1-4, DOI: 10.1109/FPL.2016.7577336
7. M. Lazzaroni, M. Brusati, A. Camplani. M. Cannon, H. Chen, M. Citterio, H. Takai, M. Wirthlin. "Tecniche Di Mitigazione Applicate A Logiche Programmabili In Ambito Di Fisica Delle Alte Energie", *XXXIII Congresso Nazionale di Misure Elettriche ed Elettrioniche*, Benevento 19 – 21 settembre 2016, ISBN: 978-88-940453-6-9, AESSE grafica srls, Settembre 2016, pp. 91 – 92.
8. M. Brusati, A. Camplani, M. Cannon, H. Chen, M. Citterio, M. Lazzaroni, H. Takai, M. Wirthlin, "An Architecture for a Mitigated FPGA Multi-Gigabit Transceiver for High Energy Physics Environments", *International Measurement Confederation (IMEKO) Workshop on Technical Diagnostics 2016: New Perspectives in Measurements, Tools and Techniques for Systems Reliability, Maintainability and Safety*, June 2016.
9. Michael Wirthlin, Andrew Keller, Chase McCloskey, Parker Ridd, David Lee, and Jeffrey Draper, "SEU Mitigation and Validation of the LEON3 Soft Processor Using Triple Modular Redundancy for Space Processing", *2016 ACM/SIGDA International Symposium on Field Programmable Gate Arrays (FPGA 2016)*, pp. 205-214, February 2016.
10. David S. Lee, Gregory R. Allen, Gary Swift, Matthew Cannon, Michael Wirthlin, Jeffrey S. George, Rokutaro Koga, Kangsen Huey, "Single-Event Characterization of the 20 nm Xilinx Kintex UltraScale Field-Programmable Gate Array under Heavy Ion Irradiation," *2015 IEEE Radiation Effects Data Workshop (REDW)*, pp.1-6, 13-17 July 2015.
11. N.A. Harward, M.R. Gardiner, L.W. Hsiao, M.J. Wirthlin, M.J., "Estimating Soft Processor Soft Error Sensitivity through Fault Injection," in *Field-Programmable Custom Computing Machines (FCCM), 2015 IEEE 23rd Annual International Symposium on*, pp.143-150, 2-6 May 2015.
12. D. Rudolph, C. Wilson, J. Stewart, P. Gauvin, A. D. George, H. Lam, G. Crum, M. Wirthlin, A. Wilson, and A. Stoddard , "CSP: A Multifaceted Hybrid Architecture for Space Computing," Proc. of the AIAA/USU Conf. on Small Satellites, Logan, UT, Aug. 2-7, 2014.
13. Lee, David S.; Wirthlin, Michael; Swift, Gary; Le, Anthony C., "Single-Event Characterization of the 28 nm Xilinx Kintex-7 Field-Programmable Gate Array under Heavy Ion Irradiation, " Radiation Effects Data Workshop (REDW), 2014 IEEE , vol., no., pp.1,5, 14-18 July 2014, doi: 10.1109/REDW.2014.7004595
14. Monson, J, Wirthlin, M, and Hutchings, B.L., "Optimization techniques for a high level synthesis implementation of the Sobel filter", Reconfigurable Computing and FPGAs (ReConFig), 2013 International Conference on, December 2013, pp. 1-6.
15. Monson, J, Wirthlin, M, and Hutchings, B. L., "Implementing high-performance, low-power FPGA-based optical flow accelerators in C", Application-Specific Systems, Architectures and Processors (ASAP), 2013 IEEE 24th International Conference on, Washington D.C., June 5-7 2013, pp. 363-369.
16. Harding, A. and Ellsworth, K. and Nelson, B. and Wirthlin, M., "Characterization and Mitigation of the MGT-Based Aurora Protocol in a Radiation Environment", Radiation Effects Data Workshop (REDW), 2013 IEEE, pp. 1-4.
17. Michael Wirthlin, Josh Jensen, Alex Wilson, Will Howes, Shi-Jie Wen, and Rick Wong, "Placement of Repair Circuits for In-Field FPGA Repair", *2013 ACM/SIGDA International Symposium on Field Programmable Gate Arrays (FPGA 2013)*, pp. 115-124, February 2013.
18. Patrick Ostler, Michael Wirthlin, and Josh Jensen, "FPGA Bootstrapping on PCIe Using Partial Reconfiguration", *International conference on Reconfigurable Computing and FPGAs (ReConFig 2011),* pp. 380-385, December 2011.
19. Nathan Rollins and Michael Wirthlin, "Software Fault-Tolerant Techniques for Softcore Processors in Commercial SRAM-Based FPGAs", *ARCS 2011 - 24th International Conference on Architecture of Computing Systems*, February 2011.
20. Josh Monson, Brad Hutchings, and Michael Wirthlin, "Fault Injection Results of Linux Operating on an FPGA Embedded Platform", *Proceedings of Reconfig 2010 International Conference on Reconfigurable Computing and FPGAs (ReConFig 2010)*, pp. 37-42, December 2011.
21. Adam Arnesen, Kevin Ellsworth, Derrick Gibelyou, Travis Haroldsen, Jared Havican, Marc Padilla, Brent Nelson, Michael Rice, and Michael Wirthlin, "Increasing Design Productivity Through Core Reuse, Meta-Data Encapsulation,

and Synthesis", *Proceedings of the 20th International Conference on Field Programmable Logic and Applications (FPL-2010)*, September 2010, pp. 538-543, DOI: 10.1109/FPL.2010.106
22. Christopher Lavin, Marc Padilla, Subhrashankha Ghosh, Brent Nelson, Brad Hutchings, and Michael Wirthlin, "Using Hard Macros to Reduce FPGA Compilation Time", *Proceedings of the 20th International Conference on Field Programmable Logic and Applications (FPL-2010)*, September 2010, pp. 438-441, DOI: 10.1109/FPL.2010.90
23. Brian Pratt, Megan Fulmer, Michael Rice, and Michael Wirthlin, "Reliable Communications Using FPGAs in High-Radiation Environments - Part I: Characterization", *IEEE International Conference on Communications (ICC 2010)*. May 2010, ISBN: 978-1-4244-6403-6
24. Nathaniel Rollins and Michael J. Wirthlin, "Fault-Tolerant Block-RAM Memories in SRAM-Based FPGAs", Proceedings of the IEEE Aerospace Conference, March 2010, Paper #1501. DOI: 10.1109/AERO.2010.5446661
25. Jon-Paul Anderson, Brent Nelson, and Mike Wirthlin, "Modified Duplicate With Compare for FPGAs Using Statistical Models for Reduced Cost Reliability", Proceedings of the IEEE Aerospace Conference, March 2010, Paper #1501. DOI: 10.1109/AERO.2010.5446660
26. Jonathan Johnson and Michael Wirthlin, "Voter Insertion Algorithms for FPGA Designs Using Triple Modular Redundancy", *2010 ACM/SIGDA International Symposium on Field Programmable Gate Arrays (FPGA 2010)*, pp. 249 – 258, February 2010.
27. Michael Caffrey, Kim Katko, Anthony Nelson, Joseph Palmer, Scott Robinson, Diane Roussel-Dupre, Anthony Salazar, Michael Wirthlin, William Howes, Daniel Richins, "The Cibola Flight Experiment", *23 Annual AIAA/USU Conference on Small Satellites*, August 2009.
28. Brian Pratt, Michael Caffrey, Paul Graham, Keith Morgan, and Michael Wirthlin, "Analysis of SEU-induced Errors in the Matched Filter of an FPGA-based Digital Communications Receiver", *19th International Conference on Field Programmable Logic and Applications (FPL-2009)*, pp. 38-43, August 2009.
29. Jonathan Heiner, Benjamin Sellers, Michael Wirthlin and Jeff Kalb, "FPGA Partial Reconfiguration via Configuration Scrubbing", *19th International Conference on Field Programmable Logic and Applications (FPL-2009)*, pp. 99-104, August 2009. (**Top 20 FPL Paper Award - 2015**).
30. Benjamin Sellers, Jonathan Heiner, Michael Wirthlin, and Jeff Kalb, "Bitstream Compression Using Partial Reconfiguration", *19th International Conference on Field Programmable Logic and Applications (FPL-2009)*, pp. 476-480, August 2009.
31. Adam Arnesen, Nathaniel Rollins, and Michael Wirthlin, "A Multi-Layered XML Schema and Design Tool for Reusing and Integrating FPGA IP", *19th International Conference on Field Programmable Logic and Applications (FPL-2009)*, pp. 472-475, August 2009.
32. Michael Caffrey, Michael Wirthlin, William Howes, Daniel Richins, Diane Roussel-Dupre, Scott Robinson, Anthony Nelson, and Anthony Salazar, "On-Orbit Flight Results from the Reconfigurable Cibola Flight Experiment Satellite (CFESat)", *IEEE Symposium on Field Programmable Custom Computing Machines (FCCM 2009)*, pp. 3-10, April 2009.
33. Brian Pratt, Michael Caffrey, Derrick Gibelyou, Paul Graham, Keith Morgan, and Michael Wirthlin, "TMR with More Frequent Voting for Improved FPGA Reliability, " *Proceedings of the International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA 2008)*, pp. 153-158, July 2008.
34. Brent Nelson, Michael Wirthlin, Brad Hutchings, Peter Athanas, and Shawn Bohner, "Design Productivity for Configurable Computing", *Proceedings of the International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA 2008)*, pp. 57-66, June 2008.
35. Heather Quinn, Paul Graham, Keith Morgan, Jim Krone, Michael Caffrey, and Michael Wirthlin, "An Introduction to Radiation-Induced Failure Modes and Related Mitigation Methods for Xilinx SRAM FPGAs", *Proceedings of the International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA 2008)*, pp. 139-145, June 2008.
36. Jonathan Johnson, William Howes, Michael Wirthlin, Daniel McMurtrey, Michael Caffrey, Paul Graham and Keith Morgan, "Using Duplication with Compare for On-line Error Detection in FPGA-based Designs", IEEE Aerospace, Paper 1255.
37. Jonathan Heiner, Nathan Collins, Michael Wirthlin, "Fault Tolerant ICAP Controller for High-Reliable Internal Scrubbing", *IEEE Aerospace*, Paper 1256.
38. Brian Pratt, Michael Caffrey, James F. Carroll, Paul Graham, Keith Morgan, and Michael Wirthlin, "Fine-Grain SEU Mitigation for FPGAs Using Partial TMR", 9th European Conference on Radiation and Its Effects on Components and Systems (RADECS 2007), 2007.
39. Matthew French, Li Wang, and Michael Wirthlin, "Power Visualization, Analysis, and Optimization Tools for FPGAs", *IEEE Symposium on Field-Programmable Custom Computing Machines*, pp. 185-191. April 2006.

40. Brian Pratt, Michael Caffrey, Paul Graham, Keith Morgan, and Michael Wirthlin, "Improving FPGA Design Robustness with Partial TMR", *IEEE International Reliability Physics Symposium (IRPS)*, pp. 226-232, April 2006.
41. Welson Sun, Michael J. Wirthlin, and Stephen Neuendorffer, "Combining Module Selection and Resource Sharing for Efficient FPGA Pipeline Synthesis", *2006 ACM/SIGDA International Symposium on Field Programmable Gate Arrays (FPGA 2006)*, pp. 179-188, February 2006.
42. Michael J. Wirthlin, "Senior-Level Embedded Systems Design Project Using FPGAs", Proceedings of the 2005 IEEE International Conference on Microelectronic Systems Education (MSE '05), pp. 91-92, June 2005.
43. Maya Gokhale, Paul Graham, Eric Johnson, Nathan Rollins, and Michael Wirthlin, "Dynamic Reconfiguration for Management of Radiation-Induced Faults in FPGAs", 11th Annual Reconfigurable Architectures Workshop (RAW 2004), Sante Fe, NM, 2004. pp. 145 - 152, ISBN 0-7695-2132-0.
44. Michael J. Wirthlin, "Computer Systems Design Competition at BYU", *2003 Frontiers in Education, IEEE Education Society*, pp. F1F-15 – F1F-21, November 2003.
45. Michael J. Wirthlin, Eric Johnson, Nathan Rollins, Michael Caffrey, and Paul Graham , "The Reliability of FPGA Circuit Designs in the Presence of Radiation Induced Configuration Upsets", *Proceedings of the 2003 IEEE Symposium on Field-Programmable Custom Computing Machines*, pp. 133-142. April 2003.
46. W. Landaker and M. J. Wirthlin, "Multitasking Hardware on the SLAAC1-V Reconfigurable Computing System", *12th International Conference on Field Programmable Logic and Applications (FPL-2002)*, pp. 806-815, August 2002.
47. M.J. Wirthlin and B. McMurtrey, "IP Delivery for FPGAs Using Applets and JHDL", *Proceedings of the 39th Design Automation Conference (DAC)*, pp. 2-7, June 2002.
48. E. Johnson, M. J. Wirthlin, and M. Caffrey, "Single-Event Upset Simulation on an FPGA", *International Conference on Engineering of Reconfigurable Systems and Algorithms (ERSA 2002)*, pp. 68-73, June 2002.
49. M. J. Wirthlin and B. McMurtrey, "Efficient Constant Coefficient Multiplication Using Advanced FPGA Architectures", *Proceedings of the 11th International Workshop on Field-Programmable Logic and Applications (FPL)*, pp 555-564, August 2001.
50. M. J. Wirthlin, B. L. Hutchings and C. Worth, "Synthesizing Hardware from Java Byte Codes", *Proceedings of the 11th International Workshop on Field-Programmable Logic and Applications (FPL)*, pp 123-132, August 2001.
51. M. J. Wirthlin and N. Sundaramoorthy, "Measuring the Routing Costs of FPGA Circuit Components". *Proceedings of the International Conference on Parallel and Distributed Processing Techniques and Applications*, Volume I, pp 129-134, June 2000.
52. M. J. Wirthlin, S. Morrison, P. Graham and B. Bray, "Improving Performance and Efficiency of an Adaptive Amplification Operation Using Configurable Hardware", *Proceedings of the IEEE Workshop on FPGAs for Custom Computing Machines*, pp. 267-275, April 2000.
53. M. J. Wirthlin and B.L. Hutchings, "Improving Functional Density Through Run-Time Constant Propagation", *1997 ACM/SIGDA International Symposium on Field Programmable Gate Arrays*, pp. 86-92, February 1997.
54. M.J. Wirthlin and B.L. Hutchings, "Sequencing Run-Time Reconfigured Hardware with Software", *1996 ACM/SIGDA International Symposium on Field Programmable Gate Arrays*, pp. 122-128, February 1996.
55. M.J. Wirthlin and B.L. Hutchings, "A Dynamic Instruction Set Computer", *Proceedings of the IEEE Workshop on FPGAs for Custom Computing Machines*, pp. 99 - 107, April 1995. (**Top 20 FCCM Paper Award**).
56. M.J. Wirthlin and B.L. Hutchings, "DISC: The Dynamic Instruction Set Computer", *Field Programmable Gate Arrays (FPGAs) for Fast Board Development and Reconfigurable Computing*, John Schewel, Editor, Proc. SPIE 2607, pp. 92-103 (1995).
57. B.L. Hutchings and M.J. Wirthlin, "Implementation Approaches for Reconfigurable Logic Applications", *5th International Workshop on Field Programmable Logic and Applications*, pp. 419-428, August 1995.
58. M.J. Wirthlin, K.L. Gilson, and B.L. Hutchings, "The Nano Processor: A Low Resource Reconfigurable Processor", *Proceedings of the IEEE Workshop on FPGAs for Custom Computing Machines*, pages 23-30, April 1994.

Conference Publications, Abstract Review

1. Brent Nelson, Michael Wirthlin, and Yubo Li, "Reliability Models for SEC/DED Memory with Scrubbing in FPGA-based Designs", Proceedings of European Radiation Effects on Components and Systems Conference (RADECS), September 2012.
2. Brent Nelson, Michael Wirthlin, Kevin Ellsworth, Alex Harding, Colby Ballew, and Travis Haroldsen, "Radiation Testing of FPGA-Based High-Speed Serial Communication", Proceedings of European Radiation Effects on Components and Systems Conference (RADECS), September 2012.

3. Heather Quinn, Paul Graham, Keith Morgan, Zachary Baker, Michael Caffery, Dave Smith, Michael Wirthlin, and Randy Bell, “Flight Experience of the Xilinx Virtex-4”, Proceedings of European Radiation Effects on Components and Systems Conference (RADECS), September 2012.
4. Nathan Rollins and Michael Wirthlin, " Fault-Tolerant Block-RAM Memories in SRAM-Based FPGAs," *Proceedings of the IEEE Aerospace Conference*, Mar. 2010.
5. W. Kunzler, Z. Zhu, M. Wirthlin, R. Selfridge, S. Schultz, A. Propst, K. Peters, M. Zikry, "High repetition-rate full-spectrum interrogation of FBG sensors for dynamic measurements in composite laminates," Proc. SPIE, vol. 7293, Mar. 2009.
6. Nathaniel Rollins, Adam Arnesen, and Michael Wirthlin, “An XML Schema for Representing Reusable IP Cores for Reconfigurable Computing”, *Proceedings of the 2008 National Aerospace and Electronics Conference (NAECON 2008)*, July 2008.
7. Wesley Kunzler, Zixu Zhu, Richard Selfridge, Stephen Schultz, Michael Wirthlin, “Integrating Fiber Bragg Grating Sensors with Sensor Networks”, *IEEE AUTOTESTCON*, September 2008.
8. Wesley Kunzler, Jason Newman, Daniel Wilding, Richard Selfridge, Stephen Schultz, Michael Wirthlin, and Andres Rodriguez, “Miniature MAV Telemetry Using a Portable Integrated FOS System”, *Proc. SPIE 6530 -- Sensor Systems and Networks: Phenomena, Technology, and Applications for NDE and Health Monitoring*, Paper 653005, 2007.
9. Michael J. Wirthlin and Welson Sun, "DSynth: A Pipeline Synthesis Environment for FPGAs", *IEEE Symposium on Field-Programmable Custom Computing Machines* (short paper), pp. 343-344. April 2006.
10. Matthew French, Paul Graham, Michael Wirthlin, and Li Wang, "Cross Functional Design Tools for Radiation Mitigation and Power Optimization of FPGA Circuits", Earth Science Technology Conference, NASA, Washington D.C., June 2006.
11. Brian Pratt, D. Eric Johnson, Michael J. Wirthlin, Michael Caffrey, Keith Morgan, and Paul Graham, “Improving FPGA Design Robustness with Partial TMR”, *8th Annual International Conference on Military and Aerospace Programmable Logic Devices (MAPLD)*, September 2005.
12. Matthew French, Paul Graham , Michael Wirthlin, Li Wang, Gregory Larchev, “Radiation Mitigation and Power Optimization Design Tools for Reconfigurable Hardware in Orbit”, Earth Science Technology Conference, NASA, Washington D.C., June 2005.
13. Nathan Rollins, Michael J. Wirthlin, Michael Caffrey, and Paul S. Graham, “Evaluation of Power Costs in Applying TMR to FPGA Designs”, 7th Annual International Conference on Military and Aerospace Programmable Logic Devices (MAPLD), Washington D.C., 2004, Paper P136.
14. D. Eric Johnson, Keith S. Morgan, Michael J. Wirthlin, Michael Caffrey, and Paul S. Graham, “Persistent Errors in SRAM-based FPGAs”, 7th Annual International Conference on Military and Aerospace Programmable Logic Devices (MAPLD), Washington D.C., 2004, Paper P135.
15. M. French, P. Graham, and M. Wirthlin, “Design Tools for Reconfigurable Hardware in Orbit”, NASA Earth Science Technology Conference 2004, Palo Alto, CA, June 22-24. ISBN 0-9721439-6-3.
16. Nathan Rollins, Michael Wirthlin, Paul Graham, and Michael Caffrey, “Evaluating TMR Techniques in the Presence of Single Event Upsets”, *6th Annual International Conference on Military and Aerospace Programmable Logic Devices (MAPLD)*, Paper P63 September 2003.
17. Michael J. Wirthlin, Nathan Rollins, Michael Caffrey, and Paul Graham, “Hardness by design techniques for field-programmable gate arrays”, *Proceedings of the 11th Annual NASA Symposium on VLSI Design*, Coeur d’Alene, ID, pp. WA11.1-WA11.6, May 2003.
18. Paul Graham, Michael Caffrey, Michael Wirthlin, Eric Johnson, and Nathan Rollins, “Reconfigurable Computing in Space: From Current Technology to Reconfigurable Systems-On-a-Chip”, *24th Annual IEEE Aerospace Conference*, Vol. 5, pp. 5:2399-5:2410, March 2003.
19. Nathan Rollins, Michael J. Wirthlin, Michael Caffrey, and Paul Graham, “Reliability of Programmable Input/Output Pins in the Presence of Configuration Upsets”, *5th Annual International Conference on Military and Aerospace Programmable Logic Devices (MAPLD)*, Paper C3, September 2002.
20. Michael Caffrey, Paul Graham, Eric Johnson, and Michael Wirthlin, “Single-Event Upsets in SRAM FPGAs”, *5th Annual International Conference on Military and Aerospace Programmable Logic Devices (MAPLD)*, Paper P8, September 2002.

Patents

1. Michael J. Wirthlin, “Automated circuit triplication method and system”, U.S. Patent Number US14308471, January 26, 2016.

2. Michael J. Wirthlin and Brad L. Hutchings, “Dynamically-Configurable Digital Processor Using Method for Relocating Logic Array Modules”, U.S. Patent Number 6,173,434, January 2001.

Presentations and Posters

1. Wirthlin, M.J., Harward, N.A.; Gardiner, M.R.; Hsiao, L.W.; "Estimating Soft Processor Soft Error Sensitivity through Fault Injection," in *Field-Programmable Custom Computing Machines (FCCM), 2015 IEEE 23rd Annual International Symposium on* , vol., no., pp.143-150, 2-6 May 2015
2. Helio Takai and Michael Wirthlin, “Accelerator Radiation Environment and the Use of FPGAs in those Environments”, *International Conference on Military and Aerospace Programmable Logic Devices (MAPLD),* May 2015.
3. Michael Wirthlin, “Accelerator Radiation Environment and the Use of FPGAs in those Environments”, *International Conference on Military and Aerospace Programmable Logic Devices (MAPLD),* May 2015.
4. Michael Wirthlin, “Neutron Radiation Test Results of the Linux Operating System Executing within the CHREC Space Processor (CSP)”, *International Conference on Military and Aerospace Programmable Logic Devices (MAPLD),* May 2015.
5. M. Wirthlin, “A Unique Fault Injection System for Estimating MicroBlaze Design Reliability on Xilinx V5QV FPGAs”, *International Conference on Military and Aerospace Programmable Logic Devices (MAPLD),* May 2014.
6. P. Gauvin, J. Urriste, C. Wilson, C. Morales, A. Stoddard, A. Wilson, A. George, G. Crum, M. Wirthlin, H. Lam, “CSP: A Multifaceted Hybrid System for Space Computing”, *International Conference on Military and Aerospace Programmable Logic Devices (MAPLD),* May 2014.
7. Alex Harding and Michael Wirthlin, “Single Event Upset Mitigation for MGT-Based Aurora Protocol in a Radiation Environment”, *International Conference on Military and Aerospace Programmable Logic Devices (MAPLD),* April 2013.
8. Michael Wirthlin, Yubo Li, and Brent Nelson, “Modeling the Scrub Rate for SEC/DED BRAMs in FPGA Circuits”, *International Conference on Military and Aerospace Programmable Logic Devices (MAPLD),* April 2013.
9. Michael Wirthlin, “Modeling the Scrub Rate for SEC/DED BRAMs in FPGA Circuits”, *International Conference on Military and Aerospace Programmable Logic Devices (MAPLD),* April 2013.
10. Brent Nelson, Michael Wirthlin, and Joe Walker, “SERET: A Tool for Weibull Curve Fitting and Space Error Rate Estimation”, *International Conference on Military and Aerospace Programmable Logic Devices (MAPLD),* April 2013.
11. Brian Pratt, Michael Wirthlin, Michael Caffrey, Paul Graham, and Keith Morgan, “Analysis of SEU-induced Errors in an FPGA-based Digital Communications System”, *International Conference on Military and Aerospace Programmable Logic Devices (MAPLD),* September 2008.
12. Patrick Ostler, Michael Caffrey, Derrick Gibelyou, Paul Graham, Keith Morgan, Brian Pratt, Heather Quinn, Michael Wirthlin, “FPGA System Error Rate Analysis for Harsh Radiation Environments”, *International Conference on Military and Aerospace Programmable Logic Devices (MAPLD),* September 2008.
13. Brian Pratt, Michael Wirthlin, Paul Graham, Keith Morgan, and Severn Shelly, “Improving FPGA Reliability in Harsh Environments Using Triple-Modular Redundancy with More Frequent Voting”, Military and Aerospace FPGA and Applications (MAFA), November 2007.
14. Jonathan Heiner, Nathan Collins, and Michael Wirthlin, “Correcting Single-Event Upsets Using Self-Hosting Partial Dynamic Reconfiguration”, Military and Aerospace FPGA and Applications (MAFA), November 2007.
15. Michael Wirthlin, “Computing with FPGAs”, Hybrid Computing Conference 2007, University of Utah.
16. M. Wirthlin, D. Poznanovic, P. Sundararajan, A. Coppola, D. Pellerin, W. Najjar, R. Bruce, M. Babst, O. Pritchard, P. Palazzari, G. Kuzmanov, “OpenFPGA CoreLib Core Library Interoperability Effort”, Reconfigurable Systems Summer Institute, July 2007.
17. Michael Wirthlin, Dan McMurtrey, Brian Pratt and Keith Morgan, “A Comparison of TMR With Alternative Fault Tolerant Design Techniques for FPGAs”, *2007 ACM/SIGDA International Symposium on Field Programmable Gate Arrays*, poster presentation, February 2007.
18. Joshua D. Engel, Keith S. Morgan, and Michael J. WirthlinPoster: “A Methodology for Estimating On-orbit Static Single Event Upset Rates Using CREME96”, 9*th Annual International Conference on Military and Aerospace Programmable Logic Devices (MAPLD)*, September 2006.
19. Matthew French, Michael Wirthlin, and Paul Graham, Poster: “Reducing Power Consumption of Radiation Mitigated Designs for FPGAs”, 9*th Annual International Conference on Military and Aerospace Programmable Logic Devices (MAPLD)*, September 2006.

20. Nathan Rollins and Michael J. Wirthlin, Poster: "Reducing Energy in FPGA Multipliers Through Glitch Reduction", *8th Annual International Conference on Military and Aerospace Programmable Logic Devices (MAPLD)*, September 2005.
21. Matthew French, Li Wang, Tyler Anderson, and Michael J. Wirthlin, Poster: "Integrated Tool Suite for Post Synthesis FPGA Power Consumption Analysis", *8th Annual International Conference on Military and Aerospace Programmable Logic Devices (MAPLD)*, September 2005.
22. Michael J. Wirthlin, invited presentation, "Reliable Spatial Computing", *1st Annual Distributed Embedded Computing Conference*, Sante Fe, NM, June 2005.
23. Michael J. Wirthlin, Invited Tutorial, "Evaluating Soft Errors in FPGAs", *IEEE International Reliability Physics Symposium*, April 2004.
24. Paul Graham, Michael Caffrey, Michael Wirthlin, D. Eric Johnson, and Nathan Rollins, Poster: "SEU Mitigation for Half-Latches in Xilinx Virtex FPGAs", *2003 IEEE Nuclear and Space Radiation Effects Conference*, June 2003.
25. Michael Wirthlin, D. Eric Johnson, Nathan Rollins, Paul Graham, and Michael Caffrey, Poster: "Validation of an FPGA Fault Simulator ", *2003 IEEE Nuclear and Space Radiation Effects Conference*, June 2003.
26. Michael J. Wirthlin, Trent Vandenberghe, and Devin Pratt , "JHDL Domain", presentation at the *5th Bi-annual Ptolemy mini-conference*, University of California at Berkeley, May 2003.
27. Michael J. Wirthlin, and Matthew Koecher , "JHDL Hardware Generation", presentation at the *5th Bi-annual Ptolemy mini-conference*, University of California at Berkeley, May 2003.
28. Michael J. Wirthlin, "The Effects of Upsets within the Configuration Memory of SRAM FPGAs", presentation at the *IEEE Microelectronics Reliability and Qualification Workshop*, December 2002.
29. Michael J. Wirthlin, Eric Johnson, and Michael Caffrey, "Single-Event Upset Simulation for Field Programmable Gate Arrays", presentation at the *2002 IEEE Nuclear and Space Radiation Effects Conference (NSREC 2002)*, 2002.
30. Michael J. Wirthlin, "Integrating the JHDL Design Environment into Ptolemy-II", presentation at the *4th Bi-annual Ptolemy mini-conference*, University of California, March 2001.

Externally Funded Contracts and Gifts:

National Science Foundation SHREC Center: 2017
NSF support ($150,000 x 3): $450,000
PI: Mike Wirthlin, Co-PI: Brent Nelson, Co-PI: Brent Nelson, Co-PI: Brent Nelson, 1/18-12/18
"BYU Site for SHREC I/UCRC"

Cisco Systems
PI: Michael Wirthlin, 10/2017 – 12/2018, $50,000
"Facilitating FPGA Fault Injection to Estimate SEU Sensitivity"

National Science Foundation CHREC Center: 2017
Sponsors: Los Alamos National Laboratory, Boeing, Raytheon, NASA Goddard, Lockheed Martin, National Instruments, Boeing, Cisco, Altera, and AFRL – Space Systems
Membership fees ($40k x 10): $400,000
NSF support (REU, Yearly Increment, and large site additional supplement): $96,000
PI: Mike Wirthlin, Co-PI: Brent Nelson, 1/17-12/17
"BYU Site for CHREC I/UCRC"

Cisco Systems
PI: Michael Wirthlin, 12/2016 – 10/2017, $35,000
"Evaluating the Effectiveness of pTMR with Embedded Fault Injection"

National Aeronautics and Space Administration (NASA): 2016
PI: David Long, Co-PI: Karl Warnick, Michael Wirthlin, and Brian Iverson, 5/16-5/18, $200,000
"Passive Inspection CubeSat (PIC)"

National Science Foundation CHREC Center: 2016
Sponsors: Los Alamos National Laboratory, Honeywell, Raytheon, NASA Goddard, Lockheed Martin, National Instruments, Boeing, Cisco, Altera, Xilinx, and AFRL – Space Systems
Membership fees ($40k x 11): $440,000
NSF support (REU, Yearly Increment, and large site additional supplement): $96,000
PI: Mike Wirthlin, Co-PI: Brent Nelson, 1/16-12/16
"BYU Site for CHREC I/UCRC"

National Science Foundation CHREC Center: 2015

Sponsors: Los Alamos National Laboratory, Honeywell, Sandia National Laboratory, NASA Goddard, Lockheed Martin, National Instruments, and AFRL – Space Systems
PI: Mike Wirthlin, Co-PI: Brent Nelson, 1/15-12/15, $280,000
"BYU Site for CHREC I/UCRC"

Cisco Systems
Gift to support research in Partial TMR and FPGA Reliability, $80,000 (1/2014) "Self Recovery using Algorithmic Partial TMR (A-pTMR) "

National Science Foundation CHREC Center: 2014
Sponsors: Los Alamos National Laboratory, Sandia National Laboratory, Lockheed Martin – APG, National Instruments, and AFRL – Space Systems
PI: Mike Wirthlin, Co-PI: Brent Nelson, 1/14-12/14, $240,000
"BYU Site for CHREC I/UCRC"

National Science Foundation CHREC Center: 2013
Sponsors: Los Alamos National Laboratory, Sandia National Laboratory, Lockheed Martin – SVIL, National Instruments, AFRL – Space Systems, Xilinx Corporation, and SEAKR Corporation
PI: Mike Wirthlin, Co-PI: Brent Nelson, 1/13-12/13, $320,000
"BYU Site for CHREC I/UCRC"

National Science Foundation CHREC Center: 2012
Sponsors: Sandia National Laboratory, Lockheed Martin – Space Systems Corporation, Lockheed Martin – SVIL, National Instruments, AFRL - Munitions, AFRL – Space Systems, Xilinx Corporation, and SEAKR Corporation
PI: Brent Nelson, Co-PI: Mike Wirthlin, 1/12-12/12, $295,000
"BYU Site for CHREC I/UCRC"

National Science Foundation CHREC Center:2011
Sponsors: Sandia National Laboratory, Lockheed Martin – Space Systems Corporation, Lockheed Martin – SVIL, National Instruments, AFRL - Munitions, AFRL – Space Systems, and SEAKR Corporation
PI: Brent Nelson, Co-PI: Mike Wirthlin, 1/11-12/11, $295,000
"BYU Site for CHREC I/UCRC"

Cisco Systems
Gift to support research in Partial TMR and FPGA Reliability, $40,000 (08/2010)

Sandia National Labs, U.S. Department of Energy
PI: Michael Wirthlin, 09/10-5/11, $30,000
"Virtex 5 Self Scrubbing – Contract Extension"

National Science Foundation CHREC Center:2010
Sponsors: Los Alamos National Laboratory, Sandia National Laboratory, Lockheed Martin – Space Systems Corporation, National Instruments, Rincon, NASA-Dryden, AFRL, and SEAKR Corporation
PI: Brent Nelson, Co-PI: Mike Wirthlin, 1/10-12/10, $314,931
"BYU Site for CHREC I/UCRC"

Sandia National Labs, U.S. Department of Energy
PI: Michael Wirthlin, 10/09-9/10, $48,000
"Non-Volatile Memory Review and Analysis – Contract Extension"

National Science Foundation CHREC Center: 2009
Sponsors: Los Alamos National Laboratory, Sandia National Laboratory, Lockheed Martin – Space Systems Corporation, National Instruments, L3 Communications, Rincon, NASA-Dryden, SEAKR Corporation, and Xilinx Corporation
PI: Brent Nelson, Co-PI: Mike Wirthlin, 1/09-12/09, $420,000
"BYU Site for CHREC I/UCRC"

National Science Foundation CHREC Center: 2008
Sponsors: Los Alamos National Laboratory, Sandia National Laboratory, NASA GFSC, Lockheed Martin, National Instruments, L3 Communications, Rincon
PI: Brent Nelson, Co-PI: Mike Wirthlin, 1/08-12/08, $278,275
"Brigham Young University To Join the I/UCRC CHREC Center"

Defense Advanced Research Project Agency (DARPA)
PI: Mike Wirthlin, Co-PI: Brent Nelson, Brad Hutchings, 9/07-7/08, $348,000
"Future FPGA Design Methodologies and Tool Flows"

Sandia National Labs, U.S. Department of Energy
PI: Michael Wirthlin, 9/07-8/08, $108,711

"Non-Volatile Memory Review and Analysis"

National Science Foundation
PI: Brent Nelson, Co-PI: Mike Wirthlin, 1/07-12/07, $10,000
"Brigham Young University To Join the I/UCRC CHREC Center"

Los Alamos National Laboratory, U.S. Department of Energy
PI: Michael Wirthlin, 1/07-12/09, $300,000
"Automated Design Techniques for Improving FPGA Fault Tolerance"

Lockheed Martin CE&T
PI: Michael Wirthlin, 9/06-9/07, $50,000
"Dynamic Internal Reconfigurable Technology"

Naval Undersea Warfare Center (NUWC)
PI: Steve Shultz, Richard Selfridge, and Michael Wirthlin, 5/06-10/08, $355,657
"Harsh Environment D-fiber Sensors (HEDS)"

Los Alamos National Laboratory, U.S. Department of Energy
PI: Michael Wirthlin, 1/06-9/06, $50,000
"Reliability Modeling of the Xilinx VirtexII and Virtex4 FPGAs"

Los Alamos National Laboratory, U.S. Department of Energy
PI: Michael Wirthlin, 1/04-12/06, $270,000
"Improving the Reliability of FPGA Designs through Automated Design Hardening"

Xilinx Corporation
PI: Brent Neslon, Co-PI: Michael Wirthlin, 4/04-4/05, $80,000
"Pro-Media Processor Development Kit"

National Aeronautics and Space Administration (NASA), sub-contract through USC-ISI
Sub-contract PI: Michael Wirthlin, 5/03-4/06, $150,000
"Reconfigurable Hardware IN Orbit (RHINO)"

Los Alamos National Laboratory, U.S. Department of Energy
PI: Michael Wirthlin, 1/02-12/03, $120,000
"Improving the Reliability of FPGA Designs Operating in a Space Environment"

Defense Advanced Research Projects Agency
PI: B. Hutchings, Co-PI: B. Nelson, M. Wirthlin, and D. Wilde, 1999-2002, $2,489,870
"Unified Debug Environment for Adaptive Computing Systems"

Internally Funded Projects:

Ira Fulton College of Engineering and Technology, Brigham Young University
M. Wirthlin, 2012-2013, $10,000
"Integrating FPGAs into Particle Physics Experiments"

Ira Fulton College of Engineering and Technology, Brigham Young University
M. Wirthlin, 2005, $6,500
"Optimized Retiming and Operation Selection for Reconfigurable Data-Path Architectures"

Watson Embedded Systems Laboratory, Dept. of Electrical and Computer Engineering
M. Wirthlin, 2004-2005, $12,000
"High-Level Scheduling and Mapping Techniques for Reconfigurable Datapaths"

College of Engineering and Technology, Brigham Young University
M. Wirthlin, 2000, $5,400
"Exploratory Research in Temporal Partitioning and Scheduling"

Graduate Students:

Ammon Gruwell, Masters of Science, April 2017
"High-Speed Programmable FPGA Configuration Memory Access Using JTAG"

Andrew Keller, Masters of Science, April 2017
"Using On-Chip Error Detection to Estimate FPGA Design Sensitivity to Configuration Upsets"

Nathan Harward, April 2016

"Measuring Soft Error Sensitivity of FPGA Soft Processor Designs Using Fault Injection"

Aaron Stoddard, Masters of Science, December 2015

"Configuration Scrubbing Architectures for High-Reliability FPGA Systems"

Michael Gardiner, Masters of Science, July 2015

"An Evaluation of Soft Processors as a Reliable Computing Platform"

Josh Jensen, Masters of Science, April 2015

"Preemptive Placement and Routing for In-Field FPGA Repair"

Alex Harding, Masters of Science, June 2014

"Single Event Mitigation for Aurora Protocol Based MGT FPGA Designs in Space Environments"

Nathaniel H. Rollins, Doctor of Philosophy (PhD), April 2012

"Hardware and Software Fault-Tolerance of Softcore Processors Implemented in SRAM-Based FPGAs"

Patrick S. Ostler, Masters of Science, December 2011

"FPGA Bootstrapping Using Partial Reconfiguration"

Derrick S. Gibelyou, Masters of Science, August 2011

"Automated Fixed-Point Analysis and Bit Width Selection in Digital Signal Processing Circuits using Ptolemy"

Brian H. Pratt, Doctor of Philosophy (PhD), April 2011

"Analysis and Mitigation of SEU-induced Noise in FPGA-based DSP Systems"

William A. Howes, Masters of Science, April 2011

"On-Orbit FPGA SEU Mitigation and Measurement Experiments on the Cibola Flight Experiment Satellite"

Adam Arnesen, Masters of Science, April 2011

"Increasing Design Productivity for FPGAs through IP Reuse and Meta-Data Encapsulation"

Jonathon Johnson, Masters of Science, April 2010

"Synchronization Voter Insertion Algorithms for FPGA Designs Using Triple Modular Redundancy"

Welson Sun, Doctor of Philosophy (PhD), April 2008

"Using duplication with compare for on-line error detection in FPGA-based designs"

Dan L. McMurtrey, Masters of Science, December 2006

"Using duplication with compare for on-line error detection in FPGA-based designs"

Keith S. Morgan, Masters of Science, August 2006

"SEU-Induced Persistent Error Propagation in FPGAs"

D. Eric Johnson, Masters of Science, August 2005

"Estimating the Dynamic Sensitive Cross Section of FPGA Design Through Fault Injection"

Matthew R. Koecher, Masters of Science, December 2003

"Hardware Synthesis of Synchronous Data Flow Models"

Brian J. McMurtrey, Masters of Science, April 2003

"Approaches in Web Based Design and Evaluation of Digital Circuits"

Benjamin L. Bullough, Masters of Science, August 2002

"Analysis of Field-Programmable Gate Array Implementations of Constant Coefficient Finite Impulse Response Filters"

Wesley J. Landaker, Masters of Science, August 2002

"Using Hardware Context-Switching to Enable a Multitasking Reconfigurable Computer System"

Steven E. Morrison, Masters of Science, April 2001

"Design and Performance Analysis of a Configurable Hardware Solution of an Adaptive Automatic Target Recognition Algorithm"